



FPGA System Planner

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Cadence Introduces Innovative FPGA-PCB Co-Design Solution

New Scalable Solution, Powered by Taray Technology, Can Shorten Design-In Time, Reduce End Product Cost and Mitigate Risk

SAN JOSE, Calif., May 18, 2009 –Cadence Design Systems, Inc. (NASDAQ: CDNS), the leader in global electronic design innovation, today introduced an innovative, scalable co-design solution for designing FPGAs onto PCB systems. The Cadence® OrCAD® and Allegro® FPGA System Planner shortens time to design-in today's complex FPGAs—those with large pin counts and elaborate banking and pin assignment rules—while reducing risk by delivering an automated placement-aware FPGA pin I/O assignment synthesis.

Developed by Taray, Inc. and available to Cadence customers through an OEM agreement, this exclusive joint solution offers an optimized correct-by-construction FPGA pin assignment that reduces the number of pin optimization iterations during PCB layout while reducing the number of layers required to route the FPGA on a PCB design. Allegro FPGA System Planner also shortens time for companies using FPGAs on PCB systems to emulate their ASICs through automated FPGA pin assignment.

"I tried other tools that promised to simplify the FPGA I/O complexity issue but none of these had an approach like Taray does," said Roberto Cordero, GCSD Signal Integrity TMT Lead, of Harris Corporation. "Taray's FPGA I/O synthesis technology is the only one that allows us to enter our design intent at the system level, and then it completely automates the pin assignment over multiple FPGAs all at once. The Taray technology will be a very strong addition to Cadence's portfolio."

The need among systems companies for increased data throughput along with increased functionality in their products has resulted in large pin-count FPGAs with high-speed I/Os. These FPGAs also have more advanced memory interfaces that consume much less power and address customers' desire to develop greener products. Use of such FPGAs with greater capacity, more capabilities and advanced high-speed interfaces has increased in PCBs, as well as for emulating ASICs using FPGAs on a PCB. The Cadence OrCAD and Allegro FPGA System Planner targets systems companies and IC companies who face challenges in using FPGAs on PCB Systems.

"Off-the-shelf multi-FPGA prototyping boards do not always meet the needs of designers," said Ed McGettigan, senior director of silicon hardware and applications at Xilinx, Inc. "Using this FPGA I/O synthesis technology, designers can create a new prototyping system while rapidly exploring multiple interconnect and component design alternatives much more quickly than by using typical manual methods for pin optimization."

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The technology is available in a series of scalable solutions from the OrCAD FPGA System Planner to the Allegro FPGA System Planner L, XL and GXL tiers, and is tightly integrated with OrCAD Capture, OrCAD PCB Designer, Allegro Design Entry HDL and Allegro PCB Design products. The FPGA System Planner shortens the time it takes to integrate FPGAs on a PCB, enhances FPGA performance through the optimal utilization of FPGA resources, and can reduce PCB manufacturing costs through the reduction in the number of PCB layers required to route dense, complex, large pin-count FPGAs.

"The Cadence FPGA System Planner is an innovative solution for design teams facing the challenges of integrating today's large pin-count, complex FPGAs into the PCB design flow," said Charlie Giorgetti, corporate vice president at Cadence. "This is exactly the type of technology, automation and innovation our customers expect from us to reduce design cycles and manage risks with large pin-count FPGAs on PCBs."

OrCAD and Allegro FPGA System Planner products work with the 16.2 release and are available for customers to adopt immediately. For more information, visit <http://www.cadence.com/cadence/newsroom/features/pages/feature.aspx?xml=fpga>

About Cadence

Cadence enables global electronic design innovation and plays an essential role in the creation of today's integrated circuits and electronics. Customers use Cadence software and hardware, methodologies, and services to design and verify advanced semiconductors, consumer electronics, networking and telecommunications equipment, and computer systems. The company is headquartered in San Jose, Calif., with sales offices, design centers, and research facilities around the world to serve the global electronics industry. More information about the company, its products, and services is available at www.cadence.com.

CB Distribution BV supports you as Cadence Channel Partner with all Cadence solutions, including the OrCAD products. As extension of the Cadence organisation, our staff has more than 50 years EDA experiences and is looking forward supporting you in your electronic development.

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