

Cadence Introduces Constraint-Driven High-Density-Interconnect Design Flow for PCB

Broad Array of New Features Eases Challenges of Today's PCB Designers

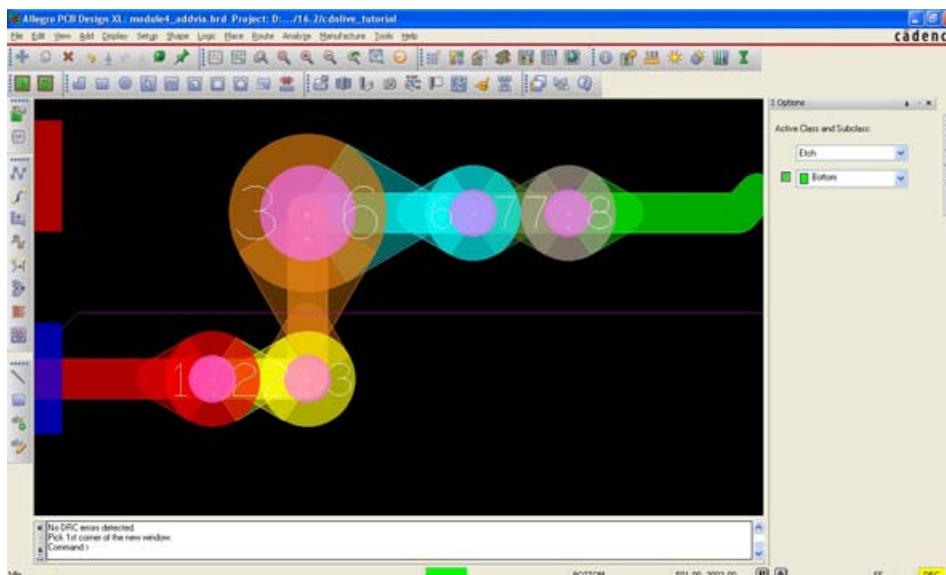
SAN JOSE, Calif., 18 Aug 2008

Cadence Design Systems, Inc. (NASDAQ: CDNS), the leader in global electronic design innovation, today announced a sweeping set of improvements to the Cadence® Allegro® and OrCAD® families of products aimed at boosting performance and productivity through new features and functionality. Part of the Cadence SPB 16.2 release, the new technology helps deliver shorter, more predictable design cycles for PCB designs. With significant improvements for designers using high-density interconnect (HDI), the technology will be of particular value to customers in the high-end consumer electronics market, as well as those in segments such as computing and networking where users are seeking a constraint-driven HDI design flow.

New technology introduced in Allegro PCB for HDI designs includes new objects, an extensive set of new rules for micro-vias, an enhanced via-transition use model, and changes to the entire PCB design flow to enable a comprehensive constraint-driven HDI design flow. Design partitioning has been enhanced with new capabilities for partitioning the design horizontally and adding soft boundaries to allow users to work in parallel more efficiently, further shortening the design cycle.

"NVIDIA designs require a PCB design solution that offers a robust constraint-driven PCB design flow," said Greg Bodi, senior manager, System Design, NVIDIA. "Having HDI capabilities that are driven by a constraint-driven flow is necessary for us to meet our time-to-market objectives. With the significant improvements for HDI designs in the Allegro PCB16.2 release, we expect to shave off up to 25 percent from the PCB layout design cycle time for our designs."

Part of the Cadence constraint-driven and automated HDI design flow, the image below shows the via-span display and dynamic fillet generation capability in Allegro PCB and IC packaging /SiP products.





Customers can shorten their time to market and reduce development costs for high-frequency signals such as those found in PCI Express 2.0, Serial ATA II, SAS II. Using Allegro PCB SI users can quickly and accurately simulate and validate for BER compliance using new and advanced eye mask capabilities, high-frequency field solver technology. In addition, Allegro PCB SI provides simulation support for interoperable, multi-vendor IBIS 5.0 AMI-compliant transceivers.

“Shrinking BGA pin pitch is forcing customers in many market segments to use high-density interconnect on their designs,” said Steve Kamin, product marketing group director at Cadence. “Cadence has excelled in constraint-driven PCB design flow for many years now, but customers also demand the HDI capability. With the significant improvements in the SPB 16.2 release, Cadence now offers both capabilities, and some of our customers already are seeing the benefits of our constraint-driven HDI design flow. These improvements, along with the many others, make this a very important release for PCB designers.”

With the layout-driven RF PCB design capability introduced in the new release, users can eliminate the need to manually update schematics for RF circuit elements added into the layout. Combined with an improved bi-directional integration with Agilent’s ADS environment, the Allegro PCB RF option allows users to shorten time to create mixed-signal digital-analog-RF designs.

The SPB 16.0 release made a significant investment in improving the ease of use of Allegro and OrCAD PCB Editor. The new release continues this emphasis on improving ease of use for all products in the Allegro family, from design creation tools in the front end to PCB layout tools in the back end.

OrCAD Capture boasts productivity and usability improvements including an updated GUI, enhanced search capabilities and new capability for designing-in FPGAs. New FPGA design-in features include the ability to create split symbols, import and export FPGA pin assignments for leading FPGA vendors tools, and ease-of-use improvements for supporting the ECO process for FPGAs.

Finally, engineers can specify and embed physical and spacing constraints for critical high-speed nets in the design to improve chances of first-time success while eliminating traditional error-prone verbal, email and spreadsheet-based communication. This can help shorten design cycles and eliminate unnecessary iterations between hardware designers and PCB layout designers.

SPB 16.2 will be available in Q4 2008.

About Cadence

Cadence enables global electronic design innovation and plays an essential role in the creation of today's integrated circuits and electronics. Customers use Cadence software and hardware, methodologies, and services to design and verify advanced semiconductors, consumer electronics, networking and telecommunications equipment, and computer systems. Cadence reported 2007 revenues of approximately \$1.6 billion, and has approximately 5,100 employees.

CB Distribution supports you as Cadence Channel Partner with all Cadence solutions, including the OrCAD products. As extension of the Cadence organisation, our staff has more than 50 years EDA experiences and is looking forward supporting you in your electronic development.

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