This document describes the new features and enhancements in Cadence® Allegro® and OrCAD® products in release 17.2-2016 Quarterly Incremental Release (QIR) 4. The products covered are:

- **Allegro PCB Editor, Cadence SiP Layout, and Allegro Package Designer** on page 2
- **OrCAD Capture** on page 92
- **PSpice** on page 93
- **Allegro Design Entry HDL** on page 95
- **Allegro EDM** on page 100
- **Allegro Pulse** on page 113
- **Allegro Constraint Manager** on page 117
This section describes the new features and enhancements in the Cadence® layout editors; Allegro® PCB Editor, Cadence® SiP Layout, and Allegro® Package Designer in release 17.2-2016 QIR 4. If a feature is available in only one or more layout editors, a note is provided mentioning the tools.

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In-Design DFx

Note: Available only in PCB Editor.

For PCB designs, design for manufacturing flow has traditionally consisted of creating fabrication data at the end of the design, which is then sent to the fabricator. Hours, or days later, the fabricator sends back a list of issues to be addressed. The issues are corrected, and the cycle of data creation is repeated, resulting in lost days in the design to fabrication phase.

Realizing this time delay between the design center and fabrication, design centers create an internal sign-off group to shorten the manufacturing cycle by bringing fabrication validation tools into their own environment. This process reduces the data to manufacturing cycle time, but not necessarily the number of cycles between the tools. Fabrication data still needs to be generated and imported into the validation tool, and a list of issues is returned to the designer for correction. This current model is, more aptly, named verify for manufacturing.

In-Design DFx in PCB Editor improves the process even further by putting fabrication checks into the constraint management system of PCB Editor. Manufacturing issues realized during the editing process can immediately be corrected rather than waiting for hours, or days, without generating manufacturing data and sorting through a list of violations from another tool. The sign-off phase still exists using tools, such as the Allegro®/OrCAD® Manufacturing Option, but with In-Design DFx, the iterations and the time required to produce fabrication data decreases multiple times.

![Figure 1-1 Conventional Design for Fabrication Flow](Image)

![Figure 1-2 In-Design DFx Design for Fabrication Flow](Image)
In-Design DFx Environment

In-Design DFx consists of bare-board fabrication checks that are defined as constraint sets in *Constraint Manager*. The Design for Fabrication (DFF) constraint set rules are assigned to the conductor and mask layers of a single stackup design, or in the case of rigid-flex, multiple stackup definitions. For layers not typically defined in the stack-up, such as silkscreen, subclasses can be grouped together by film record selection or individual class/subclasses selections to which DFF rule checks are applied. The DFF rules can be exclusively exported to a constraint or technology file for use in other designs. You can create various rule sets to address fabrication classes, design technology, or for specific manufacturers.
In-Design DFx checks are enabled or disabled in the Analysis Modes dialog box under the new *Design For Fabrication* category as shown in the following image. In this form, each DFF category may be fully enabled, or each check may be specifically selected for checking.

![In-Design DFF Checks in Analysis Modes](image)

**Figure 1-3 In-Design DFF Checks in Analysis Modes**

**In-Design DFx Checks**

*Constraint Manager* contains a new *Manufacturing* worksheet, which is divided into two categories, *DFF CSet* and *Design*. You define a CSet in the *DFF CSet* and assign to stackup layers in the *Design* category.
Design for Fabrication CSets

Each Manufacturing Design for fabrication category consists of five major subcategories:

- **Outline**

  Checks the spacing of design objects to the Board Geometry/Design_outline and Board Geometry/Cutout subclasses. Values for these rules identify issues for the spacing of traces, pins, vias, and other non-signal geometry to the board outline. The legacy Board Geometry/Outline is not considered in the checks.

- **Mask**

  Defines the rules for minimum mask slivers width and square areas of mask islands for the areas where mask material may be too small for proper adherence to the substrate.

- **Annular Ring**

  Defines the size requirements for padstack definitions for hole to pad and pad to mask size relationships for pins and vias.
Copper Spacing

Defines the rules for the minimum manufacturing spacing allowed between trace, shape, pin pad, via pad, non-plated hole, and non-signal geometry objects.

Silkscreen

Defines the rules for the spacing between pin pads, via pads and non-plated holes to silkscreen geometry. You can also specify minimum character width and minimum line width values in this rule set.

DFF Rule Creation

To create DFF rules definition, specify a name and a usage type. The usage types available are displayed in the following image:

- Etch: Define rules that are applied to the conductor and plane layers as defined in the Cross Section Editor.
- Non-Etch: Define rules that are applied to non-conductor layers such as solder mask, coverlay, and silkscreen.
- Stack-up: Define rules that are non-layer specific such as cutout to outline checks and aspect ratios.
After entering a name and usage type, the rule entry is created and only those fields associated with the usage type become enabled for value assignment.

**Note:** When assigned to the design layers, DFF rule fields that do not contain a value are not checked regardless of the enable or disable setting in the constraint modes.

Assignment of DFF CSet rules are made in the *Design for fabrication* – *Design* category. In each of the five subcategories, rule names are applied to the various layers using a pull-down menu selection. The rules listed in the pull-down menu are based on the rule usage type assignment and layer type.
When the rule assignment is made to a layer, the rule values are displayed in the form. Creating a group of non-conductor layer, such as a silkscreen layer, right-click the Not in stackup field and choose Add SubClass Group from pop-up.
The *Create subclass group* form opens. Entering a name for the subclass group, selects the subclasses based on the film records, or by individual subclass selected, then applies a rule set to the subclass group.
After all the rules are defined and assigned, they are immediately applied to PCB Editor. For violations, the DRCs are displayed in real time.

**Figure 1-4 Trace to outline violation**

**Figure 1-5 Silkscreen to via pad violation**

**Allegro Venture PCB Designer and In-Design DFx Checks**

*Allegro Venture PCB Designer* contains a broad set of technology-based layout design features. The In-Design DFx capabilities within Venture PCB Designer are expanded to address additional DFF checks and analysis that complement the technology-based features.
The In-Design DFx features in this scheme are a more granular level of features; for example, pin pad checks. In the basic version, pin pads are treated as an entity regardless of pin type. Pin pads are broken into specific types, such as thru hole pin pad, SMD Pin pad, and so on.

The more detailed objects available provide a deeper level of fabrications checks while in the design process. The following image provides an example of an expanded outline to pin checks.

**Figure 1-6 Expanded outline to pin checks**

More examples of expanded features include exposed trace area for mask opening, fiducial pad checks, silk screen text under components, and so on.

Two subcategories are also added to the Design for fabrication CSet and Design categories:

- **Holes**: Defines aspect ratio for plated pin and via. You can define maximum number of layers for skip via in this subcategory.
Copper Features: Defines values for minimum line width, minimum text line width, copper line width aspect ratios, shape to pad ratios, radius corner checks, fillet, thermal pad, antenna checks in this category.

In-Design DFx Features

All the features available in *Constraint Manager* such as copy and paste are available in the Design for fabrication rule definitions. Other common capabilities are also supported, for example:

- Double-click any column header to expand/collapse columns
- Click to sort through the column header
- Right-click the header to enable/disable *Analysis Mode*

A unique feature exclusively available in the *Manufacturing* domain is the ability to view how the rules forms are displayed. With a Design for fabrication sub-category opened in
**Constraint Manager**, choose View – Transpose View. The table view changes from the standard horizontal view to a vertical view.

**Figure 1-7** Standard (horizontal) view

**Figure 1-8** Transposed (vertical) view

In-Design DFx also provides you a method of developing various sets of Design for fabrication rules that may be targeted to specific design technologies, manufacturing classes, or specific manufacturers. In-Design DFx in PCB Editor returns the verify for manufacturing design back into the design for real design for manufacturing.
DRC Browser

The layout editors now include an advanced tool that enhances the ability to locate, review, and address DRCs. The DRC Browser UI contains various navigation, sorting, and filtering capabilities making it easier to focus on resolving design issues by DRC violation types and areas. The DRC Browser provides feedback on the number of errors, including bar and pie charts that are dynamically updated as issues are corrected or introduced, while editing the design.

The DRC Browser assists in correcting issues by providing:

- Windowing into the location of a selected DRC
- A tristate status of DRC violations (Read, Unread, Review)
- Various navigation methods
- The ability to assign the waive DRC attribute to a selected DRC
- Various filtering and sorting methods
- A DRC Chart to see a graphical representation of where to resolve the issue
DRC Browser Navigation

Choose Tools – DRC Browser to launch DRC Browser.

The DRC Browser display all DRCs created by the DRC system including external DRCs. From this browser, you have various ways to navigate through the DRCs.

- **DRC Tree** – In the DRC tree window of the form, you can expand and collapse nodes and branches of the DRC domains, down to the list of DRC locations. Each node of the list displays the number of DRCs that are present.

- **Bread Crumb Trail** – Selecting an item in the Bread Crumb navigation path assists you in quickly navigating to a previous location along the current DRC Domain. Navigation arrows may also be used to move along the most recent DRC Domain path.
List Navigation – Selecting entries in from the list navigate down to the next level or constraint rules down to the list of DRC locations.

Navigation may also be performed through the DRC Chart. The DRC Chart provides two chart types: bar and pie chart. The DRC may be used to graphically visualize and compare the number of DRCs through different domains and domain levels to aid you in focusing in
different areas of DRC violation numbers. These charts may also be used to navigate through the different DRC domains by selecting the segment of interest.

Figure 1-9  DRC Bar Chart
DRC Browser Filtering

When reviewing DRCs, *DRC Browser* provides various filtering and sorting capabilities. While in the list of DRC locations, the current list may be sorted from low to high value by selecting the column title with a click.

Filtering options include:

- List item state using the All, Unread, or Review radio buttons
- Text string
Value and numerical formulas

Figure 1-11  Filter options

Figure 1-12  Formula
Filtering is also enabled through the DRC Chart. When *DRC Chart* is displayed at the DRC list level, slide bars may be used to filter the DRC List for values between upper and lower ranges for DRC list display.
DRC Browser Features

The DRC Browser provides a description, image, DRC character code, and other details for each DRC rule when applicable.

You can also set a waive DRC as well as mark the state of a DRC as Read, Unread, or Review within the DRC location list. These states may be quickly recognized by a user-defined color scheme. When a DRC row is selected in the list, the PCB Editor window is centered around the DRC, highlighting the DRC marker and associated object, saving time in trying to locate
the issue manually. When the issue is corrected, the DRC list dynamically updates, removing the DRC from the list.

With several options available for reviewing, filtering, and the dynamic list updates, the new DRC Browser assists in quickly and efficiently locating and addressing critical DRCs in a design.

MCAD Collaboration Environment

The MCAD Collaboration environment streamlines the ECAD/MCAD flow for IDX, reducing the concern for managing the multiple changes and modifications that occur during the design cycle. This environment is based on a shared repository where both the layout editor and MCAD tools read and write IDX files. The MCAD Collaboration environment:

- Monitors the IDX repository
- Notifies if there are new updates
- Notifies pending feedback requests on PCB created changes
- Imports updates in the order they are deposited
- Eliminates the need to navigate file structures to locate the updated files
Invoking Collaborative Environment

When launching the collaboration environment from the Tools – MCAD Collaboration menu, the MCAD Collaboration docking form is opened and may be placed in the mini-status form as a tabbed form, along the layout editor frame, or outside of the editor window. Once the location of the repository is defined, and the polling interval is set through the Setup button, you can view if any updates are ready for import. When an update is present the designer is notified by a color change in the update icon as well as a pop-message stating a file is ready for import.

Importing MCAD Data

When you click the Updates button, the IDX import tool launches, loads the pending updates (no need to navigate the system to locate the file), and the incoming changes are displayed in the MCAD Collaboration form. The designers preview the import list, accept and/or reject proposed changes from the MCAD tool.

Pushing MCAD Updates

Once Apply is clicked, the accepted updates are instantiated into the design and the feedback data is written to the IDX repository for the MCAD tool to review.
Modifications are sent to MCAD when you click the *Push Updates*. The items to be sent to MCAD are displayed in the export list displayed in the *MCAD Collaboration* form for verification. Optional comments may also be added in the Global messaging window, or for any individual proposed change. When *Apply* is selected, the updates are saved to the IDX repository for the MCAD tool to receive.

The MCAD Collaboration environment provides a better experience for the PCB designer with updated notification and change management while working between the ECAD and MCAD domains, without the challenges of searching for files, import order, and update notification.
Sigrit Technology Driven High-Speed Signal Analysis and Checking

Note: Available in PCB Editor with the PCB *High Speed* option.

Allegro® Integrated Analysis and Checking is a new, unique environment blending the best of Allegro® and Sigrit™ technologies that provides analysis and checking capability entirely within the PCB Editor framework. For rule checking, DRC and ERC capabilities continue to depend on Constraint Manager as the single cockpit.
This release introduces two new workflow analysis capabilities for impedance and coupling. The workflows provide guided access to Sigrity analysis with results returned as dockable tables and plots, or as new Vision overlays.

This release also includes new DRC functionality and enhancements, which are described in subsequent sections.

**Licensing**

The minimum requirement to access the functionality is either the High Speed product option with Allegro® PCB Designer or the OrCAD Sigrity ERC product.

**Impedance Analysis Workflow**

This Analysis workflow provides impedance data feedback based on Sigrity analysis by either running an analysis or loading pre-existing Sigrity analysis results. Impedance Analysis can be either *Net Based* - Net, XNet, Bus, Differential Pair - or *Directed Group* - connections between a start component and end component(s). Analysis results display trace segment or sub-segment canvas color coding reflecting impedance values. In addition, an impedance color gradient bar with sliders is provided to filter impedance values on the canvas, and a detailed impedance results table to filter/sort by net name and impedance values.
Workflow Manager

To switch to the Impedance Analysis mode, choose *Analyze – Workflow Manager*, and select *Impedance Workflow* from the pull-down menu.
There are two Analysis modes that can be used to select objects for analysis:

- Net Based
- Directed Groups

**Net Based Analysis Mode**

The red X indicates that no nets have been selected for analysis. Select the *Select Nets* link to add nets for impedance analysis.
The XNet/Net Selection dialog box lets you view, filter, or select Flat (nets) or Hierarchical objects, such as netgroups, differential pairs, and XNets and move them to and from the Selected XNet/Nets pane.

You also have the option to view/filter/select Hierarchical objects (net groups, differential pairs and Xnets) and move them to/from the Selected XNet/Nets pane.

After clicking the OK button in the XNet/Net Selection dialog, a green check next to Select Nets link activates the Start Analysis link.

Click the Start Analysis link to begin impedance analysis. A progress meter appears under the Analysis section to track the simulation process. After the simulation completes, a green
check appears next to *Start Analysis* and the links under the *View Results* section are enabled.

If differential pairs are part of the simulation, you have the option to display the *Single Ended* impedance results or the *Diff Pair* impedance results in both the Table and the Vision.

**Impedance Table**

Select the *Impedance Table* link to display a dockable spreadsheet. The *Simulation Results* pane includes a *Summary Table* section with results for all of the selected nets. This data can be sorted by selecting any column header. Selecting a row in the *Summary Table* populates the *Detailed Table* section for further sorting on the specific trace data for
the net. You can select the rows in the *Detailed Table* section to zoom or center the canvas on the impedance variance for investigation.
Impedance Vision

Select the *Impedance Vision* link under the *Workflow Manager* to display trace segment or sub-segment canvas color coding reflecting impedance values. For more detailed impedance information, hover the mouse over a trace segment.
The color gradient bar with sliders can be used for impedance filtering on the canvas. In this case, displaying the lower reference plane reveals that traces are running over plane split which changes the impedance value.

Directed Groups Analysis Mode

Select the Select Directed Groups link to add nets for impedance analysis.

The Directed Group Selection dialog lets you view, filter, or select Nets by their connected components to create individual group(s) for selective analysis. Selecting a reference
designator on the left pane updates the right pane with its connected components for selection to form the Directed Group.

After verifying and adjusting the net selections between the two components, click the Create button to save the Directed Group to the upper pane.

The Directed Groups option can be disabled or enabled on a per simulation basis. After clicking the OK button from the Directed Group Selection dialog, a green check appears next to Select Directed Groups which activates the Start Analysis link.
After the analysis is complete, selecting Directed Group under View Modes in the View Results section of the workflow enables the Impedance Plot link. The active group name is also displayed.

**Impedance Plot**

Selecting the *Impedance Plot* link opens a dockable Simulation Plot pane. This plot uses Distance from Start on the x-axis as determined in the Directed Group definition. The Bar/Expanded tab in the plot can be filtered using the options on the right-hand side while the Scatter/Collapsed tab offers a local view. Both tabs support datatips.
Coupling Analysis Workflow

Coupling Analysis provides critical coupling feedback based on Sigrity analysis by either running an analysis or loading pre-existing Sigrity analysis results. Coupling Analysis can be either Net Based or Directed Group similar to Impedance Analysis flow. Analysis results display trace segment or sub-segment canvas color coding reflecting coupling issues. For detailed coupling information, hover the mouse over a trace segment. In addition, a coupling coefficient color gradient bar is provided with sliders for filtering on the canvas, and a detailed coupling results table to filter or sort by net name and coupling related results.

Workflow Manager

To display and dock the Workflow Manager, choose Analyze – Workflow Manager, and select Coupling Workflow from the pull-down.

Similar to Impedance Workflow, there are two analysis modes that can be used to select objects for analysis: Net Based and Directed Groups. The workflow steps are the same as the steps for Impedance Workflow.

The following steps are specific to the Coupling workflow:

- Click the Analysis Options link to define the coupling analysis parameters.
- Detect and model the coplanar traces – Enable/Disable
  - Default: Disabled
- Coupling – Trace coupling minimum net-level coupling coefficient in percentage
  - Default: 2%
- Rise Time – Trace coupling minimum coupled length in ps
  - Default: 100ps
- GeoWindow – The geometric window value for aggressor inclusion based on the user-selected victim (focus) nets. The geometric window value is used to scan for any existing...
nets (segments) within the provided distance of the selected victim nets. These nets are then considered as aggressors to the victim nets.

- Default: 0 (base value is converted based on database units)

After clicking the OK button in the **Coupling Analysis Parameters** dialog, click the **Start Analysis** link to begin coupling analysis. After the simulation completes, a green check appears next to **Start Analysis** and the links are enabled in the **View Results** section of the workflow.

You can display **Worst Case** or **Victim Results**. These settings impact the Coupling Table, Coupling Vision, and Coupling Plot presentation.

- Worst Case: Displays the maximum coupling coefficient for all segments.
■ Victim: Displays all aggressor segments for a specific victim net.

**Coupling Table**

Similar to Impedance Table, Coupling Table includes a Summary and a Detailed section. Worst Case and Victim modes differ in the way aggressors are color coded in the table. Selecting rows in the Detailed Table section to zooms or centers the canvas on the coupling issues for investigation.

**Coupling Vision**

Select the Coupling Vision link under the Workflow Manager to display trace segment or sub-segment canvas color coding reflecting coupling issues with hover over datatips for more
detailed information. The color gradient bar with sliders can be used to filter coupling coefficient on the canvas.

The **Worst Case** mode provides an overlay where the worst case coupling for any two segments on the selected nets is displayed on the canvas. In the Victim mode, the selected victim net is displayed and only its aggressors are color coded on the coefficient gradient.
Directed Groups Analysis Mode

The procedure to create Directed Groups is the same as that for the Impedance Workflow. Similarly, selecting Directed Group in the View Modes enable the Coupling Plot link.

Coupling Plot

Selecting the Coupling Plot link opens the Simulation Plot window, which also contains both the Bar/Expanded and the Scatter/Collapsed tab. The Scatter/Collapsed plot can be used to quickly identify outliers.
Impedance DRC Vision

The new Impedance DRC Vision option provides impedance data feedback based on the Allegro constraints system. Nets with an impedance constraint assigned to them display trace segment color coding that indicates adherence to impedance constraints. As you move the mouse over a trace segment, a tooltip displays the status of impedance constraints adherence as, lower, meets, or greater. Color coding can guide you to areas of concern. Making adjustments to address impedance issues dynamically updates the color coding so that you can view the interim results.

When the impedance constraints have been defined on critical nets, open Electrical Analysis modes and enable Impedance DRC to use the Impedance DRC Vision. Proceed to display and dock the new Visions manager located in the Views – Visions, menu and select Impedance DRC Vision from the pull-down menu.

Select the Modify Selection button in the Visions pane then window select nets for impedance review. Only nets with impedance constraints are color coded.
Graphical Overlays

Cline color coding identifies impedance issues based on the trace width, distance to the (ideal) reference plane driven by reported impedance DRCs. The datatip displays the details of the variance.

Differential Pair DRC Enhancements

There have been changes to the way differential pair members are checked by the Allegro constraint system. At times standard design rules do not apply to the members of a differential pair which requires them to be checked differently from non-differential pairs. Enhancements have been made to the way Static Phase is calculated. It now includes via transitions when checking back to Driven Pins and specific spacing constraints, to control the minimum spacing between the vias of the members of a differential pair.

Static Phase Control at Via Transitions

Default Static Phase DRC calculates the phase length from the Receiver Pins back to its designated Driver Pins. When the static phase constraint value is exceeded a DRC marker is reported at the Driver Pin. A new optional behavior will now perform the static phase length calculations from each differential pair via transition back to its designated Driver Pins, and report a DRC marker when the constraint value is exceeded. Any via type transition, thru, bb via, and micro will be checked as long as the differential pair members are transitioned from the same layer.
Enable DRC Condition

To activate the new check, open the Electrical Analysis modes form and expand All differential pair checks then “Enable static phase at vias options” to change the static phase DRC behavior. This mode will be disabled by default to preserve the static phase checks behavior on the existing designs. After the DRC update is completed, review the Differential Pair Phase Tolerance DRCs in the design. DRC markers are generated at the via locations when the static phase violates the constraint value checks back to the Driver Pin. The Constraint Manager DRC worksheet will include -Via as a suffix in the Object column for phase violations which are checked back from a via transition.

Evaluation Tip

Hovering over the DRC Marker will report the required Phase Tolerance value and actual value in the datatip window.
Resolving Phase Issues

To resolve phase issues at the via transitions, it is recommended to first resolve the standard Driver Pin to Receiver Pins DRCs, and then address the Driver Pin to Via Transition DRCs to avoid moving back and forth between different checks. After the standard Driver Pin to Receiver Pins DRCs are resolved, you can quickly resolve the Via Transition DRCs by using the Phase Tune command.

Intra-Differential Pair Spacing Rule

A new Referenced Spacing CSet column has been added to the Physical Domain – Net and Region worksheets to allow the assignment of a specific Spacing constraint set to drive the minimum clearance between the via members of a differential pair. This Spacing CSet does not affect the spacing between the clines of the differential pair.

Assigning the CSet

In Constraint Manager, open Physical domain and select the Net – All Layers worksheet. The Referenced Spacing CSet can be applied at the Net Class, Diff Pair, and Net/XNet objects.
This Spacing CSet can be applied in the Net and Region worksheets of the Physical domain, but cannot be referenced in a Physical CSet.

Any Spacing CSet available in the Spacing domain can be set as the Referenced Intra-DP Spacing CSet. Use of the Display – Constraint command is a quick way to view the resolved
spacing constraint. For example, in the following illustration, the \texttt{cns show} command reports the resolved spacing clearance between two differential pair vias.

![Illustration of spacing constraint](image)

**Return Path DRC**

Return Path issues may be considered an electrical problem but, in reality there are a number of physical factors in the design that can contribute to current return path. Locating these return path issues can be tricky and requires close investigation to identify the location of the problem. Waiting to perform the analysis until the design is complete may greatly affect the schedule and delay the release of the product. To address, this a new Return Path DRC has been created to locate current return path issues based on selection criteria specified in Constraint Manager. This functionality will generate DRC markers on the canvas and provide detailed analysis results in Constraint Manager.

**Licensing**

Return Path DRC is available in the High Speed option with Allegro PCB Designer, SiP Layout XL, and Allegro Package Design L (using SiP Layout XL).
Enable DRC Condition

To activate the new check, open the Electrical Analysis modes and enable the Return Path option in the Batch DRC mode to begin checking for Return Path issues. This is a unique DRC as it is limited to a batch update. You will need to use the DBDoctor utility to update this class of DRC.

Navigating Constraint Manager

Open Constraint Manager Electrical domain and select the Return Path worksheet under the Net workbook. Return Path rules can be applied directly to a Net/XNet object or to hierarchical objects, such as net groups, differential pairs, and so on. Return Path rules can also be specified as part of an Electrical CSet so that they are applied when the Electrical CSet is assigned.
Rule Descriptions

Reference Net(s) List of nets that should be considered as valid plane reference for the net where the constraint is assigned

Reference Layer Provides guidance to the DRC system to determine which layer to search for a plane reference for each cline on the routing layer. Options are Closest Plane, Dual Plane and Table.

Table Provides the ability to identify where a particular routing layer should find its reference plane at the design level.

Ignore Layer(s) Routing layer to be ignored during Return Path checking.

Length Ignore Allowable length that a cline can exist without a plane reference before generating a Return Path DRC.

Max Pad Gap Allowable length that a cline can be exposed from its plane reference when connecting to a pad before generating a Return Path DRC. Cline length is calculated from the center of the pad to the edge of the adjacent reference plan void.

Return Path DRC Example 1

- Closest reference layer is based on the spacing between the shape reference and the routing layer (dielectric thickness), which is used for Return Path checking.

- Pad Gap reports the length of the cline before the reference is achieved.
- Void Crossing reports when routing cross plane opening or when an incorrect reference is found. (1.5V reference layer plane found followed by a GND reference plane)

DRC Markers are generated on the canvas with expanded analysis results reported in Constraint Manager based on Return Path rules to the Closest reference layer.

<table>
<thead>
<tr>
<th>Objects</th>
<th>Reference Net(s)</th>
<th>Reference Layer(s)</th>
<th>Ignore Layer(s)</th>
<th>Length Ignore</th>
<th>Pad Gap</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Max</td>
<td>Actual</td>
</tr>
<tr>
<td>NGr DDR3_BYTELANE0 (10)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>NGr DDR3_BYTELANE1 (10)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>NGr DDR3_BYTELANE2 (10)</td>
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<td></td>
<td></td>
<td></td>
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</tr>
<tr>
<td>DPr DP_DDR3_DQS3</td>
<td></td>
<td>GND Dual</td>
<td>TOP.BOTTOM</td>
<td>25.000</td>
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</tr>
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</tr>
<tr>
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<td></td>
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</tr>
<tr>
<td>Net DDR3_DQS3</td>
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<tr>
<td>Rstt Ped Gap (334.640,-579.830)</td>
<td>1.6V,GND Closest</td>
<td></td>
<td>TOP.BOTTOM</td>
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<td></td>
</tr>
<tr>
<td>Rstt Void crossing (644.038,-599.938)</td>
<td></td>
<td></td>
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<td></td>
</tr>
<tr>
<td>Rstt Void crossing (644.020,-1156.039)</td>
<td></td>
<td></td>
<td></td>
<td>50.000</td>
<td></td>
</tr>
</tbody>
</table>

Return Path DRC Example 2

- Dual reference layers Return Path checking will search for reference layers matching the specified reference net above and below the routing layer.
 ■ Pad Gap reports the length of the cline before the reference is achieved at both sides of the connection when a reference layer is found. (GND reference layer found above)
 ■ If both planes above and below were a GND reference layer, 4 Pad Gap results will be reported.
 ■ Void Crossing reports the entire length of the cline as an incorrect reference is found (1.0V reference layer found below)

DRC Markers are generated on the canvas with expanded analysis results reported in Constraint Manager, based on the Return Path rules for the Dual reference layers.
Routing Applications

- Route Vision
- L-Comp Structures
- Route Optimization
- Route Clearance View
- Net Short Usability Improvement

Route Vision

**Note**: Available only in PCB Editor.

This release includes a dockable panel Vision Manager, which can be selected from the View menu. From the Vision Manager, you can start or stop different Vision applications including Route Vision. When Route Vision is enabled, you can configure the **Options** pane with one or many routing-based graphical overlay checks similar to Timing Vision.

Licensing

Route Vision is available in the new *Allegro Venture PCB Designer*.

Available checks

- Parallel Gap Less Than Preferred - Identifies segments with a gap less than the user-specified value.
- Non-Optimized Segs - Identifies non-optimized segments. Optimized segments have minimum line-to-line spacing and maximum pad-to-line spacing.
- Uncoupled Diff-Pair Segs - Identifies uncoupled differential pair segments. An option is provided for ignoring uncoupling at gatherings and gives more control.
- Non-Ideal Pad Entry - Identifies the locations of non-ideal pad entry. Ideal pad entry is defined as exiting/entering a pad and the next segment honoring the same-net line-to-pad constraints.
- 90 Degree Corners - Identifies segments creating a 90-degree corner.
- Min Miter/Corner Size - Identifies corner segments with miter/corner size of less than a minimum user-specified value.
- Min Seg/Arc Length - Identifies segments with length less than the minimum user-specified value.
- Min Arc Radius - Identifies arc radii that are less than the minimum user-specified value.
- Non-Arc Corner - Identifies non-arc corners.
Checks are performed in real-time and the results are listed in a sortable report that lets you quickly browse and check each item. Selecting an item centers it in the canvas while the up and down arrow keys move through the list for a quick review.

<table>
<thead>
<tr>
<th>Items</th>
<th>Layer</th>
<th>Net</th>
<th>Seg/Arc</th>
<th>Location</th>
</tr>
</thead>
<tbody>
<tr>
<td>Min Seg/Arc Length</td>
<td>L10</td>
<td>M_A_BA_0</td>
<td>Seg</td>
<td>(10126.81 2634.66)</td>
</tr>
<tr>
<td>Min Seg/Arc Length</td>
<td>L10</td>
<td>M_A_BA_0</td>
<td>Arc</td>
<td>(10147.09 2595.18)</td>
</tr>
<tr>
<td>Min Seg/Arc Length</td>
<td>L10</td>
<td>M_A_BA_0</td>
<td>Seg</td>
<td>(10186.49 542.40)</td>
</tr>
<tr>
<td>Min Seg/Arc Length</td>
<td>L10</td>
<td>M_A_BA_0</td>
<td>Seg</td>
<td>(10231.39 855.89)</td>
</tr>
<tr>
<td>Min Seg/Arc Length</td>
<td>L10</td>
<td>M_A_BA_1</td>
<td>Seg</td>
<td>(10044.05 2690.66)</td>
</tr>
<tr>
<td>Min Seg/Arc Length</td>
<td>L10</td>
<td>M_A_BA_1</td>
<td>Seg</td>
<td>(10057.83 2642.66)</td>
</tr>
<tr>
<td>Min Seg/Arc Length</td>
<td>L10</td>
<td>M_A_BA_1</td>
<td>Arc</td>
<td>(10138.95 2590.38)</td>
</tr>
<tr>
<td>Min Seg/Arc Length</td>
<td>L10</td>
<td>M_A_BA_1</td>
<td>Seg</td>
<td>(10218.92 851.53)</td>
</tr>
</tbody>
</table>

Items can be reported for the entire design or selectively based on the current canvas. Reporting the current canvas narrows down the report and helps you focus on a specific area of the design.

**L-Comp Structures**

High Speed signals require special care to maintain impedances. Inductance Compensation structures (L-Comp structures) help mitigate socket capacitance by introducing additional inductance on a pin. Selecting the new *Structure Generator* command in the *Via Structures* menu, opens a form that guides the creation of a re-usable structure.
Licensing

L Comp Structure command is available in the High Speed product option with Allegro PCB Designer, SiP Layout XL, or Allegro Package Design L (using SiP Layout XL).
Route Optimization

Optimized traces provide improved manufacturability as well as increased electrical performance. Standard bubbling results in hugging to or shoving against features at the minimum allowable spacing as defined in the constraints. With the introduction of the *Optimize in channel* option, single routes are centered while multiple routes are evenly spaced between the via and pin channel. You can define when this effect occurs by defining the channel size. You can also enable or disable this effect during bubble behavior by toggling the appropriate box in the *Add Connect* options pane.

![Route Optimization](image)

Route Clearance View

In 17.2-2016 QIR3, the Routing Clearance View was released as a new visual routing assistant that aids in estimating the space available in channels during interactive routing. There are two modes of operation: the spacing mode gives visualization of an object's spacing constraints, while the channel mode provides more accurate calculations by factoring
in trace width and feature to feature spacing. In the channel mode, the lack of a visual gap indicates insufficient space for routing.

In this release, Route Clearance View remains as an Unsupported Prototype. To enable this feature or choose the mode of operation, set the environment variable `clearance_view` from Setup – User Preferences.

**Net Short Usability Improvement**

The process of implementing Net Shorts has undergone usability improvements to provide a simple to use and easy to access user interface. This new UI can be found through pre-selecting a shape, pin, or via and then right-clicking over the object. You can then window or single select all the nets involved in the short before completing the action using the Complete Net Short pop-up menu command. Use the property edit command remove the net_short property.

**Productivity Enhancements**

The following list of features have been enhanced in different areas of the layout editors.

- Dynamic Component Alignment
- Dynamic Ratsnest Update
- Place Replicate Module Locking
- Place Replicate-Apply Enhancement
- Multi-site Copy/Paste
Create Bounding Shape
Padstack Editor XML Import/Export

Dynamic Component Alignment

The dynamic component alignment behavior with snapping guidelines is similar to Microsoft programs such as PowerPoint. Designers can perform the one-two combination of placing and aligning components real-time increasing their productivity and efficiency. Available during the Move command, the guidelines can be configured for either component origins, place bound edges, or both. You can also select, color of choice for the lines indicating the available snap points. This setting is located in the Color dialog Display folder.

Enabling or configuring this feature can be done from the Setup – User Preferences – Display – Align Guides section or from the Options pane Dynamic Alignment selection and Preferences setting. Guidelines will automatically appear only for components that are within the viewing area. The component being moved will snap to align with already-placed components, even if off grid. The snapping guide lines will appear in both the horizontal and vertical directions to match the already placed components.

Note: The dynamic alignment behavior can also be disabled during the move operation using pop-up menu Options – Dynamic Alignment. The following function key enables or disables state of the behavior.

Funckey a "pop dyn_option_select 'Options:@:Dynamic Alignment:@:Enable'"

Dynamic Ratsnest Update

The dynamic ratsnest behavior during component movement was introduced in release 17.2-2016 QIR 3. Nets that are user or system scheduled are ignored as are power and ground nets. Nets with a pin-count greater than 20 and components with a pin-count greater than 100 are also ignored to maintain performance during interactive.
In QIR 4, restrictions have been removed for nets assigned the Min Daisy Chain Ratsnest Schedule. In addition, the dynamic behavior is now integrated with the place manual command.

### Place Replicate Module Locking

**Note:** Available only in PCB Editor.

A new environment variable, *Place Replicate Lock Modules* when enabled automatically locks place replication modules during the Place Replicate Apply process. This prevents the editing of symbols and routes however the module as a group can still be moved by setting the find filter to *Group*. To unlock a module, use `property edit` to delete the locked property.

### Place Replicate-Apply Enhancement

**Note:** Available only in PCB Editor.

Using Place Replicate groups in a project was designed to make it easier to reuse similar circuitry across the design. When a change was required a simple update of one Place Replicate group will update all instances used in the database so everything is consistent without going thru a multiple copy process. The Place Replicate creation process generates a local place replicate (.mdd) file which can be applied to similar circuits in the design. If this local place replicate file is not available, the designer is required to perform a Place Replicate Update process which saves a local file so it can be reused in the design. In the QIR 4 release this is no longer required as Place Replicate has been revised to allow the selection of place replicate instances currently available in the database.

Place Replicate requires invoking the “Placement Edit” application mode. To leverage this enhancement, perform a Show Element of an existing place replicate group that you would
like to reuse. Be sure to enable “Groups” in the Find Filter and take note of the Instance Name in the report.

Select the components you would like to apply the Place Replicate group, hover over one of the selected components, right-click, and choose *Place replicate apply – From Database – CR_CLOCK_GEN_1*. Note the new option, *From Database* that allows you to select any
Place Replicate instance in the design so it can be applied; no local place replicate file required.

Multi-site Copy/Paste

Originally released in 17.2-2016 QIR3, the Copy command saved selected objects to a buffer for use at multiple destinations later. Pre-selected objects were then able to have the buffered objects pasted to them through a right click command.

New to QIR4 are two enhancements to copy/paste. The first is a dedicated Paste command, the second being the option of entering Paste automatically after copying objects. This new auto-paste functionality is available through the copy_autopaste environment variable. Enabling this variable changes the parameters/settings in the Options pane (Paste mode, Retain nets of vias, etc.) from the copy phase to the paste phase for easier access.
Pasting can now be done without the need of pre-selecting locations. Paste destinations can now be selected through place selection or through find filtered window selection.

In the above example, legacy copy behavior would have taken 14 clicks whereas the same can be achieved using one window selection using the enhancements.

In regards to buffered objects and the new dedicated paste command, required to select destinations before paste became available through the pop-up menu. Paste is now available through Edit – Paste menu and requires no pre-selected objects. Invoking the paste command lets you to paste the buffered contents to any desired locations using the methods described above.

Create Bounding Shape

Functionality for boundary based shape generation has been ported over from APD/SiP. Using the Create Bounding Shape command, you can now select pins, vias, fingers, and clines to create one or more auto-generated shapes based on the bounds of the objects selected. Shape creation can occur on multiple classes/subclasses simultaneously. Typical
applications are expected to be for use with Bond Fingers, HDI technologies, as well as RF and high-speed applications.

![HDO structure tied together with clines (red) versus with bounding shape (yellow)](image)

**Note:** If you use SiP Layout or Allegro Package Designer, note the feature updates and changes to the user interface.

**Padstack Editor XML Import/Export**

**Import XML**

In release 17.2-2016 QIR 3, new functionality was introduced into the Padstack Editor to allow the import of padstack data using an XML format (.pxml). In QIR 4, it is now possible to process multiple padstack definitions from within a single file using the -x option. For example,

```
padstack_editor -x <file_name> .pxml
```

Running the *Padstack Editor* on the command line with the –xg option on a file with multiple padstack definitions only parse the first pad stack in the input *pxml* and display the pad stack in the editor GUI. Similar behavior results from specifying the same file from the *File – Import XML* menu.

Output log files have the same base file name(s) as the *pxml* file(s). Wildcarding multiple *pxml* files produce one log per *pxml*. Multiple pad stack definitions within a single *pxml* file produces a single log file.
Export XML

In QIR 4, the ability to export an XML version of a padstack is supported using any of the following methods:

- On the command line using the `–xo <file_name>` option. For example,
  ```
  padstack_editor –xo via.pad
  ```
- On the command line using the `–xo <wildcard_file_name>` option. For example,
  ```
  padstack_editor –xo via*.pad
  ```
- Choose *File – Export XML* from Padstack Editor menus

Running the Padstack Editor on the command line with the `–xo` option read the specified pad file and exit after generating pxml file without launching the Padstack Editor.

Choosing *Export XML* from the Padstack Editor *File* menu run pad stack checks prior to prompting for an output file name (similar to saving a pad). Any warnings and/or errors found by the checks are displayed. If errors are detected, the pxml file is not saved.

If a single file is specified on the command line, or from the GUI, the pxml file contains a single padstack definition. If wildcard is used, multiple pad stack definitions are written to a single pxml file.
3D Canvas Updates

Note: Available only in PCB Editor.

In this release, 3D Canvas is still an Unsupported Prototype. This is the fourth phase of major 3D improvements planned for the new 3D Canvas with many additional features under development.

3D Canvas Features

3D Canvas functionality delivered in different releases are:

17.2-2016 Phase I

The first phase, introduced with release 17.2-2016 hotfix4, includes a graphics engine upgrade, collision detection, etch layer visibility controls, and cross-probing to the 2D canvas.
17.2-2016 Phase II

The second phase, started with release 17.2-2016 hotfix9, introduces interaction between the 2D workspace and the 3D Canvas, support for some industry-related export file types, and full layer modelling that includes mask, silk, and dielectric layers.

17.2-2016 Phase III

In the third phase, started with release 17.2-2016 hotfix16, existing features are improved and new features are included, such as preferences dialog, representation of the actual thicknesses of zones, ability to move components in the 3D space while interacting between the 3D Canvas and the 2D workspace, support for exporting 2D PDF along with export dialog, and addition of visibility layer controls for planes, masks, silk, and dielectric layers.

17.2-2016 Phase IV

In the fourth phase of the 3D Canvas, a major milestone is achieved with the inclusion of 3D transformation – also known as bending – of rigid-flex designs. You can now visualize how a multi-zoned rigid-flex design will look like in its folded state. Designers will also be able to conduct collision checks to see if any interferences exist – while the design is in the bent state. Additional QIR4 enhancements include movement of components while in a bend state, measurement of a selected path, cross-sectional views, color themes, user preference for symbol representation, coverlay support, layer stackups in the Visibility pane as well as numerous other enhancements.

The main enhancements made to 3D Canvas in this release are:

Rigid-Flex Transformation (Bending)

This QIR4 release builds upon the recently introduced Bend area capability on the 2D workspace by now allowing designers to transform – also known as bend - flex or rigid-flex designs from a flat 2D state into a transformed 3D state. Designers will now be able to visualize how their designs will look like when they are in their intended state. Designers also have the ability to add STEP models of housings and other such mechanical components to their PCB designs and check for fit and clearance issues.

In order for the bending ability to become available on the 3D Canvas, designers will have to do two things: have a design with specified bend areas and secondly, assign one area of the board as the 3D Anchor area. Bend areas were introduced to the Allegro PCB Editors in a previous release and this release sees the addition of the new Setup > Anchor 3D View
command. Once the bend areas have been assigned, designers can then specify the area of the design which must remain stationary (anchored) during the 3D transformation or bending.

Once a design has bend areas and the 3D Anchor point specified, then the transformation capability becomes available on the 3D Canvas. A simple right-click on the canvas will result in the *Bend* command becoming available.

Choosing *Bend* from the pop-up menu, results in the Options pane changing to show all of the bends in the design – as shown below. Each bend, along with its’ respective information, transformation slider and angle, is shown separately along with another slider at the bottom that acts on all of the selected bends as a group. The bends are listed and sorted using their Bend Order. The *Selected Bends* drop down allows you to quickly select bends by Bend Order or select all the bends at once. You can see bends transform (bend) by one of three methods:

- Click on the slider and drag it to the right to the percentage of the bend they wish to see transformed. Note that moving the slider all the way to the right side will result in the bend transforming 100% of its bend settings, meaning, if a bend is specified as a 90-degree bend, then it will bend to 90 degrees. Another bend may be specified as a 180-degree bend and therefore, moving the slider all the way to the right side will result in that bend folding till it is 180 degrees. The slider percentage is a reflection based on the specified values thus allowing each bend to be different.

- You can click anywhere along the slider area and the respective bend will transform accordingly to the approximate relative percentage.

- The third method allows the you to specified the desired angle in the Angle box. Note that if you enter an angle greater than the specified angle of the bend, then the transformation will stop at the specified angle. For example, if a bend has a specified angle of 90-
degrees but you enter an angle of 180, the bend on the 3D Canvas transforms only to 90-degrees.
You can revert transformations using the same three methods, but using the reverse methods – by either moving the slider to the left side, clicking at the left end of the slider tick mark area or entering an angle of 0-degrees.

Figure 1-13  Rigid-flex design in flat state
When a design is in its folded state, you can perform collision checks and move components. Note that movement of components while in the bent state is limited to planar movement only.

**Color Themes**

With this release, designers viewing their designs on the 3D Canvas now have a choice of color themes to visualize their designs. These realistic colors reflect the standard soldermask and silkscreen combinations that the majority of manufactured boards are created in. The available standard colors are black, blue, dark green, light green, purple, red, white and
yellow. You can also revert to using the design colors used on the 2D workspace or can create their own custom colors.

The preferred color can be selected and set using the 3D Canvas Setup > Preferences dialog in the Color Themes section using the drop down. This color setting will remain the same for all boards viewed in the 3D Canvas until changed.
Adding a user-defined custom color theme is done with a pop-up menu when the Color Theme drop down is in view.

New user-defined color themes are added at the end of the drop down list as shown below. Existing defaults themes cannot be modified. User-added themes can be added, deleted, copied or modified.

Measure Path

As part of this release, it is now be possible to measure between surfaces or points of the design or the STEP models in the design. You can measure between two points or multiple points – the calculations will be additive.

Measure Path is invoked by a right-clicking anywhere on the 3D Canvas. Once selected, as the cursor is moved over objects on the design, either selectable design surfaces or objects
will highlight, or tessellated (triangular) sections of STEP models will highlight. Selecting an object or surface will result in a blue dot on the 3D Canvas – to represent the point of selection and the X, Y & Z location of the selected point showing up on the Options pane.

When you select another object or surface, another blue dot will be added at the second selection point and a blue line will appear between the two selected points. This process continues for each and every multiple selection point added. Each location of the selection
points is added to the Options pane and the total accumulated distance is shown (as shown in the screen shot above).
Cutting Plane (Cross Section) Views

Have you ever wanted to peek inside a crowded assembly or look at a cross-section view of a PCB assembly? Well now with release 17.2-2016 QIR4 you can by using the new Cutting Plane feature added to the 3D Canvas Preferences dialog. Once a design is in the 3D Canvas, choose Setup – Preferences and select Cutting Plane found in the Categories section.

Turn on the Cutting Plane feature by checking on the Enable Cutting Plane setting and then selecting the alignment plane to be used for cross-section viewing – the X, Y or Z axis. Once an axis has been selected, use the Offset slider to see the effect on the 3D design. The Offset slider will move the cutting plane on the major axis selected under Alignment. The other two
available sliders allows you to angle the cutting plane in the other two opposite available axis if desired – as shown below.

Symbol Representation

In order to remove some of the visual clutter and give a choice in what you wish to see on the 3D Canvas, QIR4 introduces a symbol representation setting that lets you choose viewing either place bound shapes, STEP models, or for component representation on the 3D
Canvas. The setting can be found on the 3D Canvas under *Setup - Preferences* in the *Symbol Representation* category.

Below are representations of the components with the three settings – Place_Bound shapes only, STEP models only and the bottom example, both Place_Bound shapes and STEP models together.

**Coverlay Support**

With this release, the 3D Canvas now interprets and displays Coverlay layers properly as can be seen from the QIR3 (left) and QIR4 (right) screen shots below. We have also attempted to
graphically display Coverlay layers as visually correctly as well with the gold default color that are part of the Color Themes.

Stackup Zones (Visibility Pane)

As part of our goal for our tools to have a consistent look and feel, we have now improved upon the 3D Canvas Visibility pane and user experience by adding the Layer Stackup drop down that will be available when a PCB design has multiple stackups as part of its' cross section.

Miscellaneous Updates

QIR4 builds upon the previous releases by enhancing and refining some existing features as well as adding some new ones. Some of the changes include:

- Logical sort order for the Symbol Pane
- Text rendering improvements - Especially evident on the silkscreen layers
- Cancel processing - You can now use the ESC key to cancel invocation of the 3D Canvas
- Pin/Via plating - The correct drill size is now calculated and holes are visually shown correctly – in particular in the dielectric layers
Dielectric rendering improvements - Includes proper representation of slots, cavities, cutouts and areas created with NCROUTE_PATH and NCROUTE_PLATED

Improved progress meter - New three stage progress meter also includes starting as soon as 3D is invoked

Retained settings for Visibility/Display settings - Any display preferences or changes to the Visibility pane are now maintained between sessions

Performance improvements - 3D load times have been greatly sped up as well as the performance of the rigid-flex transformation have been improved. The bending routine was enhanced by taking advantage of multi-core/multi-threading capabilities.

New 3D Element filter - You now can use the drop-down to the right of the 3D icon to select only the objects they wish to transfer to the 3D Canvas. This feature can also be used to assist customers with large designs that may not otherwise load into the 3D Canvas by allowing them to granulize the selection to only the relevant objects.

Visibility pane improvements - Pins and vias selection/color boxes have been added to the dielectric layers on the Visibility pane to give more control of what they see on the 3D Canvas. This is especially beneficial to designers of buried and blind vias.

Allegro PCB Symphony Team Design Option

Allegro® PCB Symphony Team Design Option allows you to connect to a common database to perform collaborative design activities with each team member seeing the design updates in real time. Using this common database approach there is no need to generate or import design partitions to see the other team members’ design work. Whether a formal project team is formed or at a moment’s notice, a designer can simply share their current design and invite other designers to join.

To access this concurrent design environment requires the following products along with the Symphony Team Design product option:

- Allegro PCB Designer
- Allegro Package Design L (using SiP Layout XL)
- SiP Layout XL
The following is the list of enhancements:

**Placement Tasks**

- **Placement Edit Application mode**
  - Restore of application mode functionality without library access
- **Place Replicate support**
  - Create, Update, and Apply place replicate group
  - Apply place replicate groups created by other clients (design instance) without the need of a local place replicate (.mdd) file
- **Component Alignment**
  - Allows alignment in the Horizontal/Vertical direction and using a particular alignment edge.
  - Spacing could also be adjusted based on DFA constraints and using entered values under the Options Tab.
- **Pin Swap Support**
  - Swap pins to improve routing flow into devices by selecting pins or ratsnest closest to swappable pins.
  - Back Annotation of pin swaps to the schematic is not supported in the concurrent design environment but the Symphony session can be paused to allow back annotation to occur.

**Interactive Routing Task**

**Diff Pair Phase Tune**

- Allows the addition of single line or arc timing bumps by selecting a signal of a differential pair.
- Bump length and height can be defined under the Options Tab to add an exact size timing bump to meet phase.
Integrated Analysis and Checking

**Note:** Available only in PCB Editor.

Impedance Vision: Canvas cline color coding to identify and troubleshoot impedance related issues.

- Impedance DRC Vision: Color code clines driven by Impedance Rule requirements applied to the Nets. (DRC Marker alternative – Ideal plane)

- Impedance Analysis Vision: Color code sections of a cline driven by Impedance analysis of select nets or by loading analysis results from past simulations. Enhanced table reporting/navigation with vertical color bar for canvas display filtering (Complex plane aware)

General Tasks

- Add Line, Arc w/Radius, 3pt Arc, Circle and Text commands

- Text Edit command

Symphony Server

- Pause Session Support
  - Allows a single client exclusive access to the server database to perform activities outside of the concurrent design environment
  - The client who pauses gains full functionality of the layout editor leaving other connected clients in review mode only until the session is resumed.
  - Netlist Import, IDX Import, Pin Swapping Back Annotation, and so on.

- New multi-threaded communication architecture Improves performance by dividing server related tasks into multiple threads.
Design for Manufacturing Applications

Technology Dependent Footprints

New technology inside layout editor offers automated replacement of footprints, currently a manual process using Alternate Symbols during the move command. Whether it is retargeting footprints to accommodate mask requirements for a new manufacturing assembler, or the need to change a component's footprint when moving from a rigid to flex zone, PCB Designer no longer has to remember to use the Alternate Symbol command from the pop-up menu to make the change.

Driven from the Technology Dependent Footprint table shown in the following image, design teams can now migrate to an automated process replacing the legacy use model of alternate symbol selection during interactive placement. Moreover, this solution has no front-end dependencies other than the standard netlist. You can consider eliminating new assignments of alternate symbols in the front-end part tables in favor of an exclusive back-end driven process. By default, PCB Editor continues to support the ALT_SYMBOLS methodology but the ALT_SYMBOLS property can be used in conjunction with Technology Dependent Footprints to enable specific parts to override the mapping for a particular PACKAGE (JEDEC Type).

Licensing

Technology Dependent Footprints is licensed to the Miniaturization option and the new Venture PCB Designer or SiP Layout XL or Allegro Package Design L (using SiP Layout XL).
It is offered as an Unsupported Prototype in QIR4 for your evaluation. Enable the User Preference variable `allegro_tdp_enabled` to access the command.

Adoption Considerations

Adoption of Technology Dependent Footprints application, require some planning between the Engineering, Library, and Manufacturing teams. One should reference how they implemented the DFA Analysis table as the same strategy will apply in terms of maintaining a site table with the option for the PCB Designer to reduce the content to that matching the symbols in his/her respective database. When new symbols are created by the library team, this should trigger an entry in the table if alternate symbols are applicable. Unlike the migration steps to DFA analysis, there is no impact to the current library as this solution is intended to use existing libraries without any changes.
Smart Placement

Note: Available only in PCB Editor.

Tools to design Rigid-Flex PCBs were introduced in the 17.2-2016 base release, one of which was the auto-dropdown of components to the surface flex layers, typically, an inner layer in the database. This feature increases the productivity and does not require selection of Place on Layer command from the pop-up menu, and to set up embedded layers in the cross section. In this release, advance solution is provided with the Technology Dependent Zone-aware Footprint solution. As components are manually placed across the rigid and zone sections of the PCB Design, they are auto-interactively changed to the respective footprint of that zone.
The table below specifies a Zone Technology column called *Flex* which can map to several different named physical zones. The symbol rows shaded in yellow are those which will map the default footprints to ones ending in a FLEX suffix.

![Image of Technology Footprint Editor with zone](image15)

**Figure 1-15** Technology Footprint Editor with zone

![Image of Components placed in rigid-flex zone](image16)

**Figure 1-16** Components placed in rigid-flex zone use default package type
Key Improvements

- Alternate Package Symbol selection can now be controlled by activating the new Technology Dependent Footprint Editor available in Setup – Technology Dependent Footprints menu.

- PCB Designers are no longer required to remember to use Alternate Symbol pop-up menu command to change the default symbol to an available option in the drop-down menu.

- The mapping table accommodates top, bottom and embedded layer mapping assignments.

- Provides complete back-end solution that is independent of front-end libraries. Do not require traditional assignment of jecdec types and netlist export from the schematic tool.

- Compatible with non-Cadence schematic driven flows.

- Supports footprint requirements for physical zones, which is common with rigid-flex designs.

- Technology Dependent Footprint file promotes consistent usage across design teams and can be controlled using the path variable TECHPATH.
Miscellaneous Enhancements

- **Thieving with Hexagon Shapes**
- **Cross Section Chart and Table update**
- **IPC356 Export**
- **New Via Structure Report**
- **New Properties**
- **New ENV Variables**

**Thieving with Hexagon Shapes**

Thieving is typically added to surface layers to balance the chemical process for PCB plating. PCB Editor supports both surface, internal, and even mask layer thieving patterns. Hexagon shapes now supported in QIR 4 in addition to the legacy circle, rectangle, and line options. Enabling the *Packed spacing* option updates the spacing X and spacing Y fields providing a consistent spacing around a staggered hexagon pattern as shown in the following image.

![Hexagon Thieving with Packed Space Enabled](image)

*Figure 1-17  Hexagon thieving with packed space enabled*
Cross Section Chart and Table update

A new field *Chart Unit* in the *Cross Section Chart* dialog box permits table units to override database units.

IPC356 Export

Added new field NET for the pin/via with the NET_SHORT property.

New Via Structure Report

Via Structure report provides list of nets, via structure names, return net names, structure type, rotation, mirrored status and location.

- Generate a via structures report by net name for manual validation of via structure usage in design or as part of manufacturing collateral generation.
- Go to *Reports* and generate a quick report Via Structures by Net Report.
- You also have the option to create new extracta view file and customize via structure report.
- Interactive querying in the database can be done using *Find by Query*.
- Select via structure object and filter by net, type, net count, return net, rotation, mirror, differential pair name.
New Properties

- **IDF Exclude**
  IDF_out command ignores symbol instances with this property, use model targeted for components with DNP intent.

- **IDX Exclude**
  IDX_out command ignores symbol instances with this property.

New ENV Variables

- **Artwork_filename_prefix**
  Controls prefix on film names from environment setting.

- **Artwork_filename_suffix**
  Controls suffix on film names from environment setting.

- **Artwork_allwarnings**
  Display all warnings in the photoplot log file.

- **Backdrill_skip_pairs_question**
  Skips the backdrill pairs question if layer pairs are not initialized.

Productivity Toolbox Updates

Shield Router

- New cline shield option is available as an advanced setting. A cline shield must connect at least to one pin/via/shape assigned to a net.

- Soldermask can be enabled as an advanced setting. Size and gap can be specified in a similar way like etch layers.

- Issue with tandem voiding of static shapes resolved

- New gap value for tandem shields where value specifies the size of a user-defined void to be generated in the tandem shield along the selected cline structure.
Enhancements for Analog/RF Option of PCB Designer and SiP Layout

Enhancements have been made in PCB Designer and SiP Layout with the Analog/RF option to increase productivity in the following areas.

- Clearance Commands
- Via Array Commands

Clearance Commands

The clearance initialization and setup commands (rf_ac_init and rf_ac_setup) now supports generic shapes. A new column Shape is added to control the settings for creating clearance for generic shapes. Following image display clearance added to generic shapes in the design and Clearance Settings section of clearance command options.

By default, symmetrical clearances are created for generic shapes. The only exception are the shape that connects to two pins, which are very close to the shape boundary. For such shapes an asymmetrical clearance is created. You can, however, swap asymmetrical offset values using a context-menu command swap before placing the clearance shape.

For more information, see Working with Clearances in Allegro User Guide: Working with RF PCB.
Via Array Commands

The via array placement commands (add_bviaarray, add_viaarray, and del_viaarray) now include the following:

- Via structures placement support for differential pairs
- DRCs for via structures according to same net spacing checks
- Performance improvement during via placement.

IC Packaging-Specific Updates and Behavior Changes

Note: Available only in SiP Layout and Allegro Package Designer.

- Performance Updates
  
  ICP designers who work with big dies with more than 100K pins, will see noticeable improvements in performance with operations related to copy/paste, placement, and symbol editing.

- Fillets and the Plating Bar

  The default action of the filleting feature has been updated to add fillets to the plating bar traces by default. You can turn off adding fillets by setting pbar_trace_no_fillet in User Preferences.

- Prior to this QIR, despite turning off the visibility of wires in the design, the ETCH/WIRE subclass would often get added to the artwork film, due to the objects the wires were connected to. In this QIR, the ability to add the wires based on their visibility has been removed. If you want to add wires, use the Manufacture – Documentation – Bond Wire Documentation – Bond Wire Doc Prep command to add them to a film and include them in the output.
OrCAD Capture

This section describes the following enhancement in OrCAD® Capture in release 17.2-2016 QIR 4.

Performance Improvement

Performance has been improved for various design specific cases, such as designs with large number of netgroups.
PSpice

This section describes the following enhancements in Cadence® PSpice in release 17.2-2016 QIR 4.

- Large and complex expressions in netlists on page 93
- Enhanced numerical precision on page 93
- Improved convergence on page 93
- Generating Device Modeling Interface (DMI) independent of Visual Studio versions on page 94

Large and complex expressions in netlists

You can now create complex expressions of up to 245 characters in netlists. The length of lines in netlist has been increased from 132 to 245 characters.

Enhanced numerical precision

Numerical values can now have a higher precision as the minimum parameter value supported is $1e^{-80}$ in comparison to the earlier $1e^{-33}$.

Improved convergence

Convergence has been enhanced because of the following new controls for Pseudo Transient Analysis to handle bias point convergence:

- $PTRANABSTOL$: Determines stabilization of currents (capacitor). Default value is $1e^{-7}$.
- $PTRANVNTOL$: Determines stabilization of voltages (inductor). Default value is $1e^{-6}$.
- $PTRANSTABSTEPS$: Sets the maximum iterations to run before stopping. Default is 2100000.
Generating Device Modeling Interface (DMI) independent of Visual Studio versions

The process of Device Modeling Interface (DMI) has been enhanced with the ability to generate Device Modeling Interface (DMI) template independent of MS Visual Studio version. Use any version of MS Visual Studio to generate DMIs.
Allegro Design Entry HDL

This section describes the following enhancements in Allegro® Design Entry HDL in release 17.2-2016 QIR 4.

- Support for Data Tips on page 96
- Ability to Lock Components on page 97
- Support for Block Re-import on page 98
- Moving Off-grid Components to Grid on page 99
Support for Data Tips

Organizations might often want to provide part-specific recommendations to designers for quality purposes. You can now add these recommendations and guidelines as data tips. Designers will see these data tips in the schematic when adding components to a design.

You can define data tips in a definition file, which can be saved as a text file. Tips can be text or hyperlinks. International language support is also available.

Components with data tips have an information icon.

Designers have the option to check a box to indicate that guidelines have been followed. To verify that all guidelines have been followed, you can also generate a report.
Ability to Lock Components

There are times when a designer might not want a critical component in a schematic block to be moved or modified. This could be for various reasons. For example, multiple designers work on a design and you do not want any changes to a component. Sometimes, the circuity of a particular component is so complex that you want to minimize accidental changes.

DE-HDL now allows you to identify a component as locked so as not to allow any changes.
Support for Block Re-import

Design Entry HDL now supports the re-import of blocks which have been re-imported as read only.

The location from where the source block was imported is stored, and checked periodically for changes. DE-HDL informs the user if the source changes.

Displayed in bold if the source block changes
Moving Off-grid Components to Grid

When reusing schematics created by other users, nets or instances on the schematic could be off grid. This makes it difficult to wire these components.

To move off-grid components to the grid, you can now use a new command, _movetogrid. This command works on the currently opened schematic page.
Allegro EDM

This section describes the following enhancements in Allegro® EDM in release 17.2-2016 QIR 4.

■ Allegro Library Manager
  - Introduction of LDAP over SSL Authentication
  - Usability Enhancements in Library Import
  - Automatic Creation of Classifications of Unclassified Front-End Models and Parts
  - Footprint Set Support
  - Check out and Check in Parts with Linked Models
  - Enhancement to Link To Property
  - Release Cycle Support for Manufacturer Part Numbers

■ Allegro Data Manager
  - Dynamic Labels in Allegro Design Management
Introduction of LDAP over SSL Authentication

Lightweight Directory Access Protocol over Secure Sockets Layer (LDAPS) is now supported in Allegro EDM.

This release includes support for SSL technology that encrypts data to ensure confidentiality and security of data/traffic.

For more information on using LDAPS, see the Configuring Allegro EDM chapter in Allegro EDM Configuration Guide.

Usability Enhancements in Library Import

Until this release, librarians had to run through a series of steps outside the Library Import utility to generate missing metadata in models.

Librarians had to close the Library Import utility, then execute scripts auto-generated by Allegro EDM during pre-analysis. There was also no option to reset the metadata version.

In addition, Allegro EDM displayed errors, warnings, and information messages by default in the pre-analysis report.

Three new check boxes have now been introduced in the Library Import utility to simplify library import.

- **Generate Missing Metadata** - Generates a report of missing metadata in the libraries being imported.
■ **Regenerate All Metadata** - Removes existing metadata and recreate it. 

**Note:** Use this option with caution as regenerating metadata every time you perform pre-analysis adds extra processing time.

■ **Show Only Errors in Report.log** - Displays only error messages in the Report.log file.
Automatic Creation of Classifications of Unclassified Front-End Models and Parts

Allegro EDM now automatically classifies front-end models, such as Schematic and zero-pin Mechanical models, and parts that are unclassified in the source .csv and .cat files. These
models and parts are classified under a Library - Cell - Part Name structure. This provides an easy way to identify and search these imported models.

Models and parts that were unclassified in the category or CSV files in releases prior to 17.2-2016 QIR 4.

Unclassified models and parts are now classified in 17.2-2016 QIR 4. As can be seen, these libraries are displayed in uppercase.
Searching unclassified schematic models in releases prior to 17.2-2016 QIR 4
Unclassified models and parts in a Library - Cell - Part Name structure.

The Part Name is displayed only if the cell has associated primitives with different PTF headers.
Footprint Set Support

In Allegro EDM, footprint models have a fixed set of compatible alternate footprints that are used in a component library. The unique combination of footprints and alternate footprints can be reused with new parts.

In earlier releases, librarian had to associate footprints and alternate footprints separately to a part, which was error prone.

With this release, librarians can associate a footprint set with parts. A footprint set is a combination of footprint model and alternate footprints. To enable this feature in an existing Allegro EDM component database, Database Editor has been enhanced to automatically detect and display unique footprint sets from the database.

You can now associate these footprint sets to parts while creating or modifying parts. You can also add or delete alternate footprints in a footprint set and apply the changes to other existing parts that use the same footprint set.

For details on how to use the footprint sets, refer to Allegro EDM Database Editor User Guide.
Check out and Check in Parts with Linked Models

In this release, you have the option to check in and check out models linked to a part. Use one of the following ways to check out a part along with any of its linked models:

- Select Edit – Check-out Hierarchy.
- Right-click the part node and select Check-out Hierarchy.

You can select the associated models in the resultant Check-out Part ‘<part number>’ with Hierarchy for Modification window. Similarly, you can check in the part with its associated models by using the Check-in Hierarchy option.

For more information, refer to Allegro EDM Database Editor User Guide.
Enhancement to Link To Property

Sometimes, a PTF has many properties that are a combination of more than one property. For example, the DESCRIPTION property may be a combination of VALUE, TOLERANCE, and so on. It was difficult to manage such properties because whenever the values of VALUE or TOLERANCE were changed, the DESCRIPTION too had to be modified.

To solve this problem, the Link To property has been enhanced to use a combination of multiple properties. With this release, the Link To property in the Schematic Model Classification window lets you define the value of a particular property as a combination of other properties or attributes of a part, or model. You can also map the property to a relation.

The format that can be used is any combination of:

<SampleText>, $prop(<Model Type>.<Property Name>); <SampleText>

As an example, if you want to specify the value of DESCRIPTION as RES is 10K, 1% and 100V, the Link To dialog box needs to be edited to include the following combination:

$prop(Schematic Model.Model Name) is $prop(Part.VALUE), $prop(Part.TOL) and $prop(Part.Voltage)

When a PTF is generated, the property value is derived from the value specified in the Link To property column.
Designers can view Link To property values in Part Information Manager.

For more information, refer to Allegro EDM Database Editor User Guide.
Release Cycle Support for Manufacturer Part Numbers

Starting with this release, manufacturer parts can be checked out, edited, checked in, released, and distributed like any other part.

You can release and distribute Manufacturer Part Numbers (MPNs) using the standard library flow utilities — Data Exchange or Database Editor, and Library Distribution. To use Data Exchange for manufacturer part revisions and lifecycle support, you will have to configure it.

Check-in comments are also now supported like other non-manufacturer parts. You can also release a new version of an MPN, which will be visible to designers after library distribution.

When you uprev the component database, Allegro EDM will by default set the version of existing manufacturer parts to 1.0 and assign the Released status.

If you edit manufacturer part classifications, Database Editor will also revise the existing classifications.
As a result of these changes, when searching for MPNs in Part Information Manager, only the latest and distributed MPNs will be displayed in the search results. Allegro EDM Report Generator will also only display the latest manufacturer part revisions.

**Dynamic Labels in Allegro Design Management**

ECAD Administrators or ECAD Site Managers might sometimes want labels based on dynamic information, such as the project revision or project number.

Starting with this release, ECAD Administrators and ECAD Site Managers can define labels using variables, referred to as dynamic labels, in Allegro Design Management and Design Entry HDL. These variables serve as placeholders to display dynamic information.

Dynamic labels can be custom variables from a .cpm file, or they can be from the metadata of a Pulse project. Custom variables can be in any of the four project files — project, site, installation, or user-specific .cpm file.

After a project integrator defines and selects custom labels for a project, project team members can join a project using a dynamic label.

For more information on dynamic labels, see the *Working with Labels* section in *Allegro Design Management User Guide*. 
Allegro Pulse

This section describes the following enhancements in Allegro® Pulse in release 17.2-2016 QIR 4.

- Support Added for Multiple Sites and Multiple Web Applications on page 113
- Support Added for System Creation on page 114
- Usability Improvements in Allegro Pulse User Interface on page 114
- Ability to Compare Vendor BOM Data on page 114
- Ability to View Design Activity Log for Most Commonly-Used Data Management Functions on page 115
- Custom Metrics Enhanced on page 115
- Support Added for Dynamic Labels on page 116

Support Added for Multiple Sites and Multiple Web Applications

An enterprise may consist of multiple divisions where each division may have different requirements for data management. For example, a division may have a requirement of having separate site administrators, or, a division may want different attributes to be configured for different features, such as SPL, BOM, templates, default web parts/pages and so on. A division may also want to isolate its data from the rest of the divisions and only allow access-based permissions. Allegro Pulse supports the following two approaches to support the above requirements:

1. Separate site collections for each group
2. Separate web applications for each group

For more information, refer to the Support for Multiple Sites and Web Applications section in Allegro Pulse Configuration Guide.
Support Added for System Creation

An Electrical System contains multiple boards. Most of the organizations are interested to look at system level rolled-up BOM, system level rolled-up SPLs, system-level rolled up Vendor BOMs, system-level Issues roll-up, system-level tasks roll-up, and also system-level status, system-level column roll-ups like RoHS compliance and so on. In this release, support has been added for a system container that can store various projects from different workspaces with list roll-up to support system-level BOM, SPL, and Variant BOM.

Usability Improvements in Allegro Pulse User Interface

Starting with this release, several usability improvements have been made in the Allegro Pulse user interface.

- **Support for editing Project Template Data**: You can now edit a site/workspace, system, or project. You can perform edit operations, such as renaming a site/workspace, system, and project. In addition, you can edit the Properties, Board Details, and Users information for a project. To edit a site/workspace, system, or project select it and choose **Site – Edit**. Alternatively, right-click the site/workspace, system, or project and choose **Edit** from the context menu.

- **Support for default project and recently used projects**: You can set a project as the default project so that the selected project opens every time when you launch Pulse in a web browser. To set a project as default, right-click the project and choose **Set as Default** from the context menu.

- **Site and Workspace merged**: With the introduction of Multiple Site collection and System, workspace has been merged into site for ease of use. Now, site and workspace provide the same functionality. As a result, this functionality change has no impact on the end user.

Ability to Compare Vendor BOM Data

As a user, you may want to identify the most suitable vendor in terms of the vendor’s ability to supply the complete parts list in BOM. For this, you may want to compare the parts list from different vendors. In this release, ability compare Vendor BOMs has been added that enables you to choose the most suitable vendor based on your requirements. Currently, only Part Number attribute can be compared. Comparison of duplicate part numbers is not available.

You can also compare the data from different variant BOMs in a similar manner.

For more information, see *Comparing Vendor BOM Data in Allegro Pulse User Guide*. 
Ability to View Design Activity Log for Most Commonly-Used Data Management Functions

Analysis of design history is important to understand the kind of changes made in the design along with the information on users who have initiated the change. This information helps in analyzing the changes in the design in its life cycle. Starting with this release, Pulse creates a log for the following type design activities along with name of the user who performed the task, and the date and time when the task was performed.

- ETD
- Check-ins along with comments
- Apply/Remove/Lock/Unlock Label
- SPL Approval Initiation/Approval
- Delete Block

This information is available in standard angular grid so that you can filter the data based on date, user, activity type, and so on. In addition, you can export this data into .csv and .pdf formats.

For more information, refer to the Viewing Project Activity Logs section in Allegro Pulse User Guide.

Custom Metrics Enhanced

Starting with this release, Allegro Pulse enables you to view metrics data derived from an external source. You can now define the data in a metrics.csv file and store the file in the <design_dir>/ecw/metrics directory. Pulse automatically adds this data on the Metrics page.

For more information on custom metrics, refer to Defining and Collecting Metrics and KPIs section in Allegro Pulse User Guide.
Support Added for Dynamic Labels

ECAD Administrators or ECAD Site Managers sometimes want labels based on dynamic information, such as a design or board number.

Starting with this release, ECAD Administrators and ECAD Site Managers can define labels using variables, referred to as dynamic labels, in Allegro Pulse. These variables serve as placeholders to display dynamic information.

In Pulse, these labels can be created using project metadata. This metadata can be defined during project creation, or while editing a project. For details on creating labels using Pulse metadata, see the Customizing Project Data section in Allegro Pulse User Guide.

In ADM, these labels can be created using custom variables in .cpm files. For details, see the Working with Labels section in Allegro Design Management User Guide.

If the same variable is defined in Pulse metadata as well as Customer variable in CPM, the CPM value gets higher priority.
Allegro Constraint Manager

This section describes the following enhancement in Allegro® Constraint Manager in release 17.2-2016 QIR 4.

- Manufacturing Design for Fabrication Checks on page 118
- Static Phase DRC Enhancements on page 120
- Return Path DRC on page 122
- Intra-DP Spacing Rule on page 122
- Miscellaneous Enhancements on page 122
Manufacturing Design for Fabrication Checks

The new bare-board fabrication checks are defined as constraint sets in Constraint Manager. The Design for Fabrication (DFF) constraint set rules are assigned to the conductor and mask layers of a single stackup design, or in the case of rigid-flex, multiple stackup definitions. Constraint Manager has a new *Manufacturing* worksheet, which is divided into two categories, *DFF CSet*, and *Design*. Define Cset in the *DFF CSet* and assign to stackup layers in the *Design* category.

Each *Manufacturing Design for fabrication* category consists of the following five major sub-categories:

- **Outline** – These checks focus on the spacing of design objects to the *Board Geometry/Design_outline* and *Board Geometry/Cutout* subclasses. Values for these rules
identify issues for the spacing of traces, pins, vias, and other non-signal geometry to the board outline. The legacy Board Geometry/Outline is not considered in the checks.

- **Mask** – Defines rules for minimum mask sliver width and square areas of mask islands where mask material may be too small to for proper adherence to the substrate.

- **Annular Ring** – Defines the size requirements for padstack definitions for hole to pad, pad to mask size relationships for pins and vias.

- **Copper Spacing** – Rules for the minimum manufacturing spacing allowed between trace, shape, pin pad, via pad, non-plated hole, and non-signal geometry objects.
Silkscreen – Define the space from pin pads, via pads, and non-plated holes. Minimum character width and minimum line width values are also defined in this rule set.

<table>
<thead>
<tr>
<th>Name</th>
<th>Constraint set usage</th>
<th>Pin pad</th>
<th>Via pad</th>
<th>Non plated hole</th>
<th>Min width(line arc, shape)</th>
<th>Min length(line arc)</th>
</tr>
</thead>
<tbody>
<tr>
<td>&lt;Create new&gt;</td>
<td></td>
<td>x</td>
<td>x</td>
<td>x</td>
<td>x</td>
<td>x</td>
</tr>
<tr>
<td>Flex_Ss</td>
<td>Non-Etch</td>
<td>8.000</td>
<td>6.000</td>
<td>10.000</td>
<td>4.600</td>
<td>7.000</td>
</tr>
<tr>
<td>Rigid_Ss</td>
<td>Non-Etch</td>
<td>10.000</td>
<td>8.000</td>
<td>12.000</td>
<td>5.000</td>
<td>10.000</td>
</tr>
</tbody>
</table>

To create DFF rules definition specify a name and a usage type. The usage types are as follows:

- **Etch** – Rules that are designated to be applied to the conductor and plane layers as defined in the Cross Section Editor.
- **Non-Etch** – Rules that are applied to non-conductor layers such as solder mask, coverlay, and silkscreen.
- **Stack-up** – Rules that are non-layer specific such as cutout to outline checks and aspect ratios.

**Note:** For more information, see *In-Design DFx* section of the PCB Editor product note.

**Static Phase DRC Enhancements**

Static phase DRC calculates the phase length from the receiver pins back to the designated driver pins and reports a DRC marker at the driver pin when the static phase constraint value is exceeded.

The new, optional behavior performs static phase length calculations from each differential pair via transition back to the designated driver pins. A DRC marker is reported at the via locations when the static phase violates the constraint value checks back to the driver pin. Any via type transition that includes thru via, BB via, and micro via are checked as long as the differential pair members are transitioned from the same layer.
You can enable this new check, in the Electrical section of the Analysis Modes dialog. Expand *All differential pair checks* and select *Enable static phase at vias option* to change the static phase DRC behavior.

The Constraint Manager DRC worksheet includes -*Via* as a suffix in the Objects column for phase violations, which are checked back from a via transition.

**Note:** For more information, see *Differential Pair DRC Enhancement* section of the PCB Editor product note.
Return Path DRC

A new Return Path DRC has been created to locate return path issues based on selection criteria specified in Constraint Manager. This functionality generates DRC markers and provides detailed analysis results in Constraint Manager.

For more information, see Return Path DRC on page 47.

Intra-DP Spacing Rule

A new Referenced Intra-DP Spacing CSet column has been added in the Net and Region worksheets of the Physical domain. You can assign a specific Spacing Cset (SCset) to drive the minimum clearance between the via members of a differential pair. This SCSet does not affect the spacing between the clines of the differential pair. You can apply this SCset to Net Class, Differential Pair, Net, and XNet objects.

For more information, see Intra-Differential Pair Spacing Rule on page 45.

Miscellaneous Enhancements

Some other enhancements made to Constraint Manager includes:

- Revamped Analysis Modes Setup UI
- Techfile Import Enhancement

Revamped Analysis Modes Setup UI

In this release, user interface of Analysis Modes dialog box is remodeled. You can enable the checks and set their values at the same place. Hovering over the information icon displays the attribute name and description in the viewing pane.

For more information, see In-Design DFx on page 3.
Techfile Import Enhancement

The technology file import process has been upgraded with the following enhancements:

■ Changes in constraint values are retained when Constraint Manager is relaunched.
■ Changed constraint values are displayed in the constraint difference report.